ESESC: A Fast Performance, Power, and Temperature Multicore Simulator

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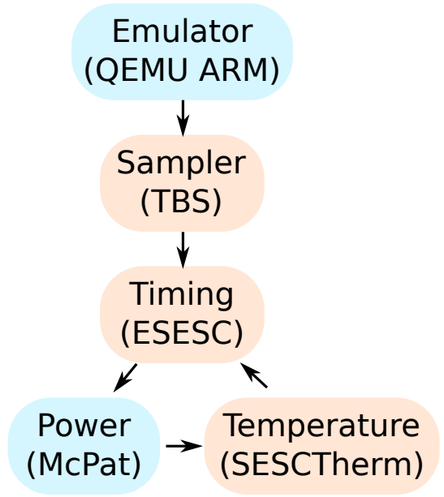
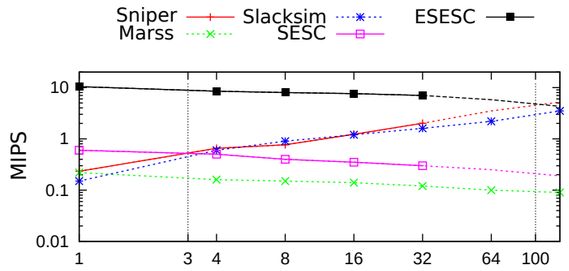
Features:
➔ISA ARM
  ➔Executes unmodified binaries
  ➔Leverages QEMU
➔Supports Time-Based Sampling
➔Detailed Performance models
  ➔Out-of-order: ROB, RAT, window...
  ➔In-order: superscalar, load-hit...
  ➔Configurable memory hierarchy
  ➔Validated against ARM Cortex A15
  ➔Multicore MOESI coherence
➔Detailed Power and Temperature
➔Open source

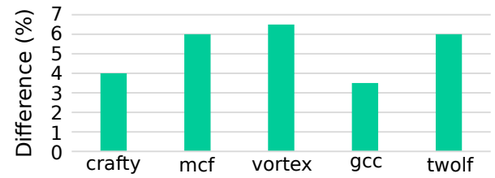
http://masc.soe.ucsc.edu/esesc



ESESC is FAST!
➔Faster than any other available cycle accurate simulator



ESESC is accurate
➔Validated against ARM A15 (chromebook)



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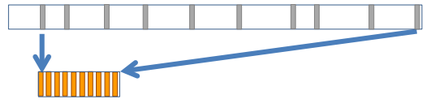
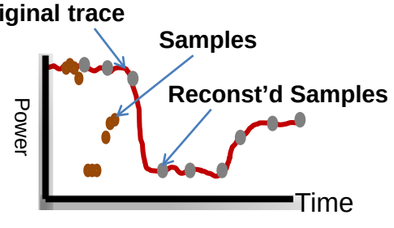
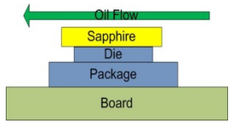
We need sampling for fast simulations
➔Select a representative subset
➔Automatic without profiling
➔Just simulate a subset of the program

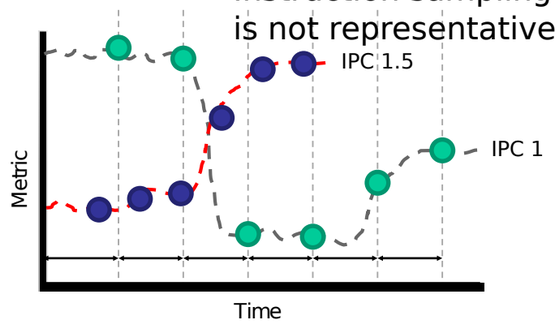


Current Sampling Problems:
➔It does not work for multithreaded
➔It does not work for temperature



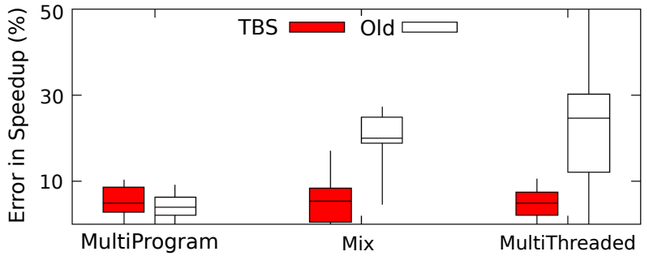


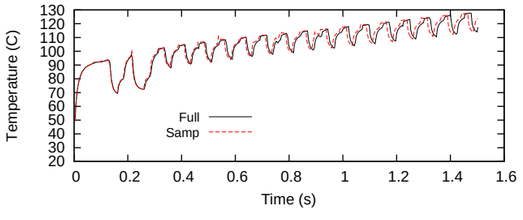
Instruction sampling is not representative

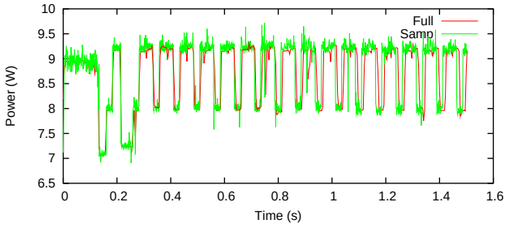


Using direct measurements, we observed that if we estimate the initial condition, we can do sampling for temperature

Time-Based Sampling (TBS):
➔Sample based on time
  ➔Not instructions as usual
➔Estimates power/time for skipped phases







References:
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